	Application No.	Applicant(s)
	10/082,372	CONNELL ET AL.
Notice of Allowability	Examiner	Art Unit
	Andre' C. Stevenson	2812
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this a or other appropriate communicati GHTS. This application is subject	application. If not included on will be mailed in due course. THIS
1. 🖾 This communication is responsive to Request for RCE filed	l on April 10, 2006.	
2. X The allowed claim(s) is/are 1-74.		•
3. A The drawings filed on 25 May 2004 are accepted by the Ex	raminer.	
<ul> <li>4. ☐ Acknowledgment is made of a claim for foreign priority un</li> <li>a) ☐ All b) ☐ Some* c) ☐ None of the:</li> <li>1. ☐ Certified copies of the priority documents have</li> <li>2. ☐ Certified copies of the priority documents have</li> <li>3. ☐ Copies of the certified copies of the priority doc</li> </ul>	been received. been received in Application No.	•
International Bureau (PCT Rule 17.2(a)).		,
* Certified copies not received:		·
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		ly complying with the requirements
5. A SUBSTITUTE OATH OR DECLARATION must be submit INFORMAL PATENT APPLICATION (PTO-152) which give		
6. CORRECTED DRAWINGS ( as "replacement sheets") mus	t be submitted.	
(a) 🔲 including changes required by the Notice of Draftspers	· · · · · · · · · · · · · · · · · · ·	O-948) attached
1)  hereto or 2)  to Paper No./Mail Date		
(b) ☐ including changes required by the attached Examiner's Paper No./Mail Date	s Amendment / Comment or in the	e Office action of
Identifying indicia such as the application number (see 37 CFR 1. each sheet. Replacement sheet(s) should be labeled as such in the		
7. DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT		
Attachment(s) 1. ☑ Notice of References Cited (PTO-892)	5. ☐ Notice of Informa	l Patent Application (PTO-152)
2.  Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Summa	
3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 04/10/06, 05/10/06	Paper No./Mail I 8), 7. ☐ Examiner's Amen	pare idment/Comment
4. ☐ Examiner's Comment Regarding Requirement for Deposit	8. 🛛 Examiner's Stater	ment of Reasons for Allowance
of Biological Material	9. 🗌 Other	11///h
		HAEL LEBENTRITT SORY PATENT EXAMINER

## Information Disclosure Statement

The information disclosure statement (IDS) submitted on 04/10/06 and 05/10/06 were filed before the first action of the merits of the requested RCE. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.

# Reasons for Allowance

The following is an examiner's statement of reasons for allowance: While the prior art teaches a method for producing a non-warped semiconductor die; however, the prior art of record either singularly or in combination failed to anticipate or render obvious the limitations of applying a stress-balancing layer to a thinned wafer to balance stress caused by a front passivation layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claims #1 through 74 are allowed.

### Claim #1

> Applying a stress-balancing layer to said wafer substantially balancing the stress caused by the front side passivation layer.

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### Claim #28

> Reducing a cross-section of said semiconductor die by thinning said semiconductor die applying a stress-balancing layer to said wafer.

### Claim #33

> Applying a stress-balancing layer to said wafer substantially balancing the stress caused by the front side passivation layer.

#### Claim # 59

> Applying a rigid stress-balancing layer to a portion of said thinned back side. said stress-balancing layer comprising a material markable with indicia.

### Claim #60

> Applying a rigid stress-balancing laver to a portion of said thinned back side.

### Claim #65

Applying a rigid stress-balancing layer to said thinned back side of the semiconductive material of the wafer under conditions which apply a back side stress generally equivalent to said front side stress of the front side passivation layer upon restoration to conditions of said semiconductor die use.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <a href="http://pair-direct.uspto.gov">http://pair-direct.uspto.gov</a>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866 – 217 – 9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre C. Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt, can be reached on (571) 272 1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 1782. Also, the proceeding number can be used to fax information;

• (703) 872-9306

Andre C. Stevenson Art Unit 2812 05/23/06

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER